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Research Interests

My research interest lies in system optimization, machine learning (ML), electronic design automation (EDA), and quantum computing. I am currently working on system optimization.

Education

University of California San Diego Ph.D. in Computer Science and Engineering

National Taiwan University

Bachelor of Electrical Engineering

Experience

IEEE Computer Architecture Letter

reviewer

University of California San Diego

PhD student

- Developed an algorithmic-neural network mixed framework for the Rectilinear Steiner Minimum Tree Problem (RSMT) to increase the scalability from 1k points of prior works to 10k points.
- Software-Hardware Co-Optimization for processing in-memory.

MediaTek

R&D Engineer

- Designed and implemented a reinforcement learning method that speeds up floorplanning by more than 3 times.
- Deployed a distributed training system of an LLM on a cluster of > 100 GPUs and sped up the system by 30x by careful profiling and reducing the critical path.
- Designed an information retrieval system by augmenting transformers to reduce the error rate by 40%.

Maxeda Technology

R&D Engineer

• Designed experiments to verify a reinforcement learning-based chip design model to justify solution quality.

National Taiwan University

Research Assistant

• Designed and developed a novel qubit mapping framework and algorithm that scales up to 20,000 qubits (only 127 in prior works).

Publications

- Andrew B. Kahng, Robert Nerem, Yusu Wang, Chien-Yi Yang. 2024. NN-Steiner: A Mixed Neural-algorithmic Approach for the Rectilinear Steiner Minimum Tree Problem. AAAI'24.
- Cheng, C., Yang, C., Wang, R., Kuo, Y., & Cheng, H. (2022). Robust Qubit Mapping Algorithm via Double-Source Optimal Routing on Large Quantum Circuits ArXiv. /abs/2210.01306
- Philipp Ennen, Federica Freddi, Chyi-Jiunn Lin, Po-Nien Kung, RenChu Wang, Chien-Yi Yang, Da-shan Shiu, and Alberto Bernacchia. FEVER'23
- Fu-Chieh Chang, Yu-Wei Tseng, Ya-Wen Yu, Ssu-Rui Lee, Alexandru Cioba, I-Lun Tseng, Da-shan Shiu, Jhih-Wei Hsu, Cheng-Yuan Wang, Chien-Yi Yang, Ren-Chu Wang, Yao-Wen Chang, Tai-Chen Chen, and Tung-Chieh Chen. 2022. Flexible chip placement via reinforcement learning: late breaking results. DAC'22.

Projects

Q_{syn}

An open-sourced quantum circuit compilation framework

• A qubit mapping framework that scales up to 20,000 qubits.

Skills

December 2021 – June 2022

September 2021 – December 2021

September 2017 – June 2021

September 2023 – present

September 2022 – present

September 2017 – June 2021

September 2022 – present